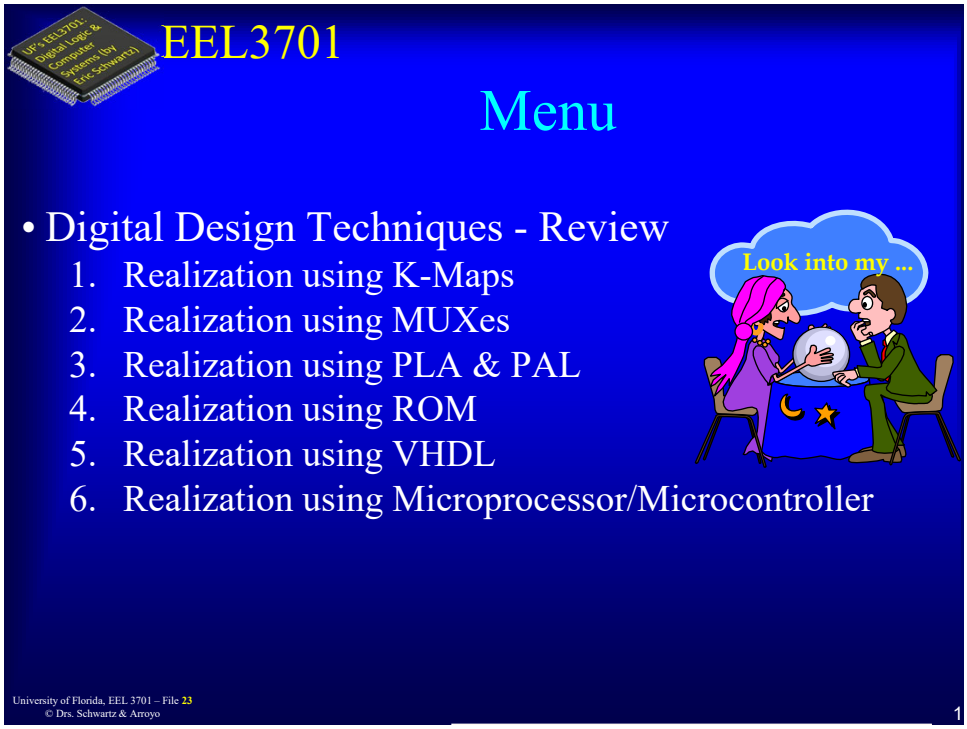
EEL3701
Menu
• Digital Design Techniques - Review
1. Realization using K-Maps
2. Realization using MUXes
3. Realization using PLA & PAL
4. Realization using ROM
5. Realization using VHDL
6. Realization using Microprocessor/Microcontroller
Look into my ...
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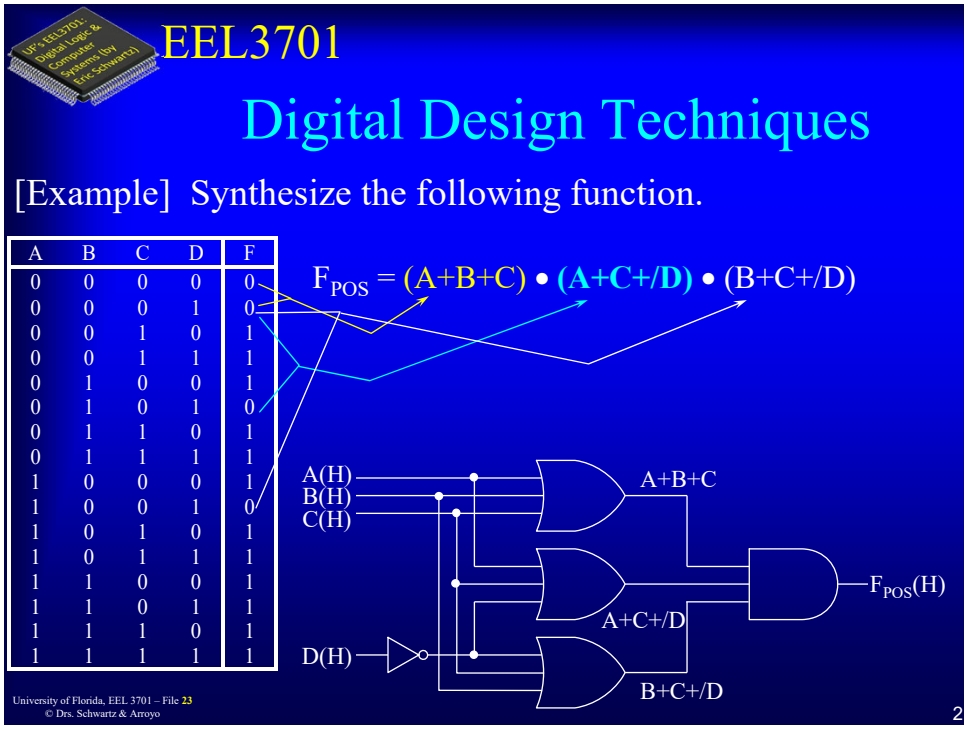
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Digital Design Techniques
[Example] Synthesize the following function.
A B C D F
0 0 0 0 0
0 0 0 1 0
0 0 1 0 1
0 0 1 1 1
0 1 0 0 1
0 1 0 1 0
0 1 1 0 1
0 1 1 1 1
1 0 0 0 1
1 0 0 1 0
1 0 1 0 1
1 0 1 1 1
1 1 0 0 1
1 1 0 1 1
1 1 1 0 1
1 1 1 1 1
$F_{POS} = (A+B+C) \bullet (A+C+/D) \bullet (B+C+/D)$
A(H)
B(H)
C(H)
D(H)
A+B+C
A+C+/D
B+C+/D
$F_{POS}(H)$
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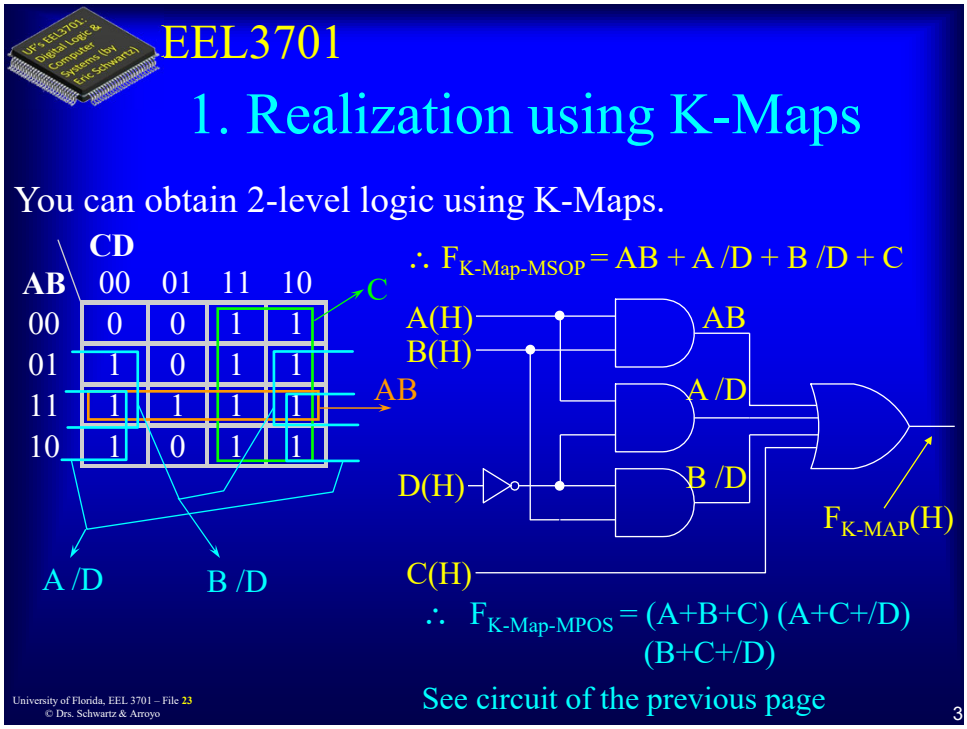
EEL3701
1. Realization using K-Maps
You can obtain 2-level logic using K-Maps.
CD
AB 00 01 11 10
00 0 0 1 1
01 1 0 1 1
11 1 1 1 1
10 1 0 1 1
C
AB
A /D
B /D
∴ F K-Map-MSOP = AB + A /D + B /D + C
A(H)
B(H)
D(H)
C(H)
AB
A /D
B /D
F K-MAP(H)
∴ F K-Map-MPOS = (A+B+C) (A+C+/D) (B+C+/D)
See circuit of the previous page
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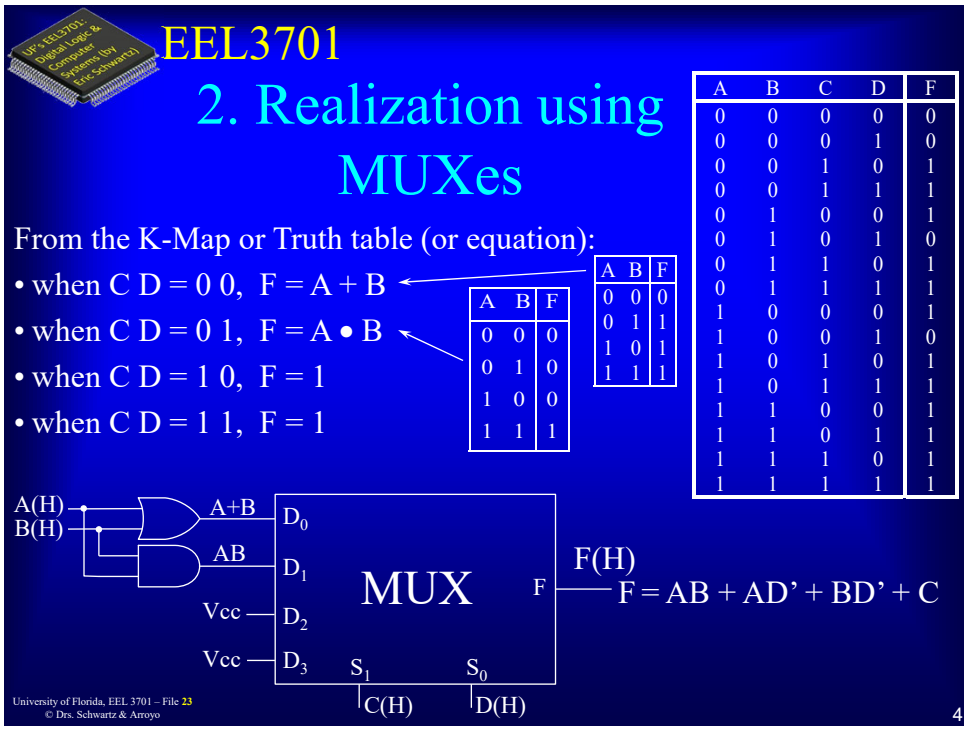
EEL3701
2. Realization using MUXes
From the K-Map or Truth table (or equation):
• when C D = 0 0, F = A + B
• when C D = 0 1, F = A • B
• when C D = 1 0, F = 1
• when C D = 1 1, F = 1
A B F
0 0 0
0 1 0
1 0 0
1 1 1
A B F
0 0 0
0 1 1
1 0 1
1 1 1
A B C D F
0 0 0 0 0
0 0 0 1 0
0 0 1 0 1
0 0 1 1 1
0 1 0 0 1
0 1 0 1 0
0 1 1 0 1
0 1 1 1 1
1 0 0 0 1
1 0 0 1 0
1 0 1 0 1
1 0 1 1 1
1 1 0 0 1
1 1 0 1 1
1 1 1 0 1
1 1 1 1 1
A(H)
B(H)
A+B
AB
Vcc
Vcc
D0
D1
D2
D3
MUX
F
S1
S0
C(H)
D(H)
F(H)
F = AB + AD' + BD' + C
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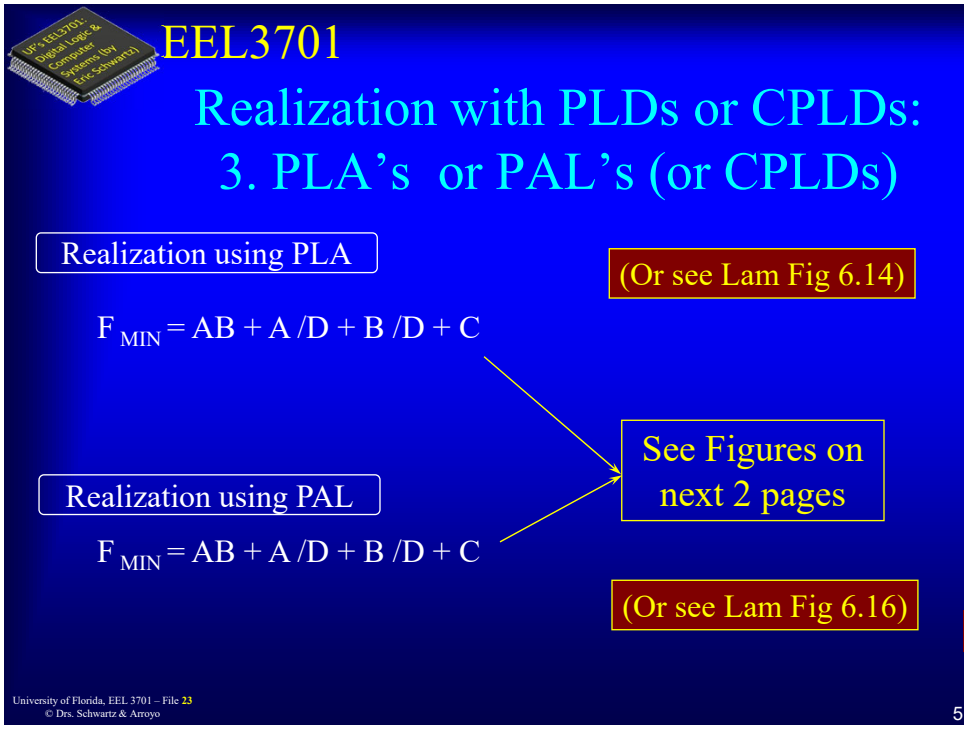
EEL3701
Realization with PLDs or CPLDs:
3. PLA's or PAL's (or CPLDs)
Realization using PLA
(Or see Lam Fig 6.14)
F MIN = AB + A /D + B /D + C
See Figures on next 2 pages
Realization using PAL
F MIN = AB + A /D + B /D + C
(Or see Lam Fig 6.16)
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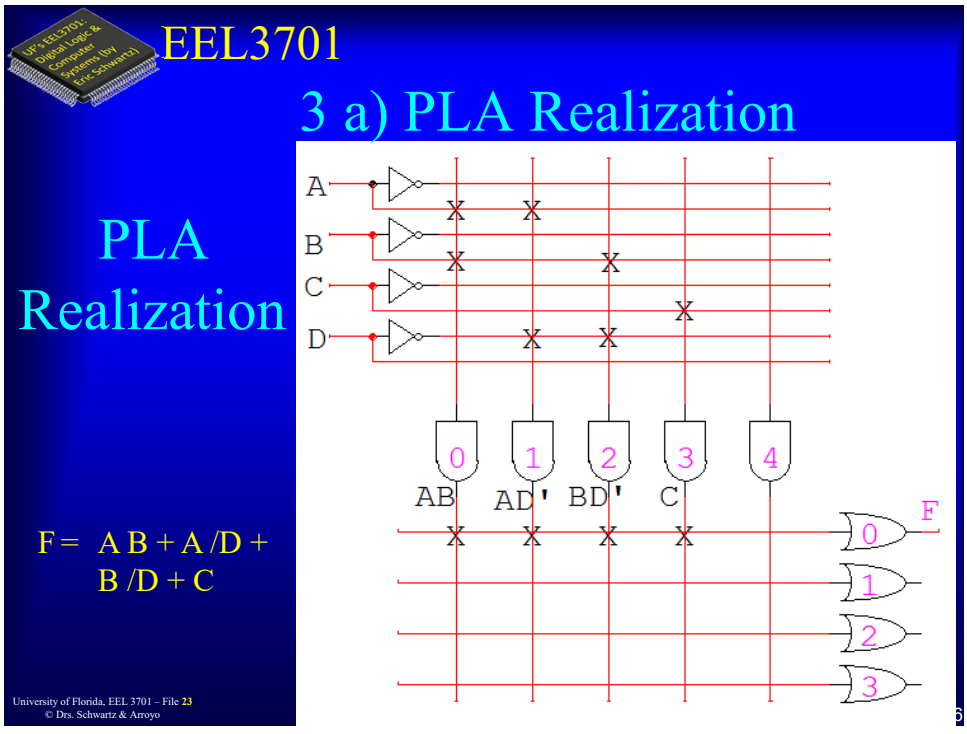
EEL3701
3 a) PLA Realization
PLA Realization
F = A B + A /D + B /D + C
A
B
C
D
0
1
2
3
4
AB
AD'
BD'
C
F
0
1
2
3
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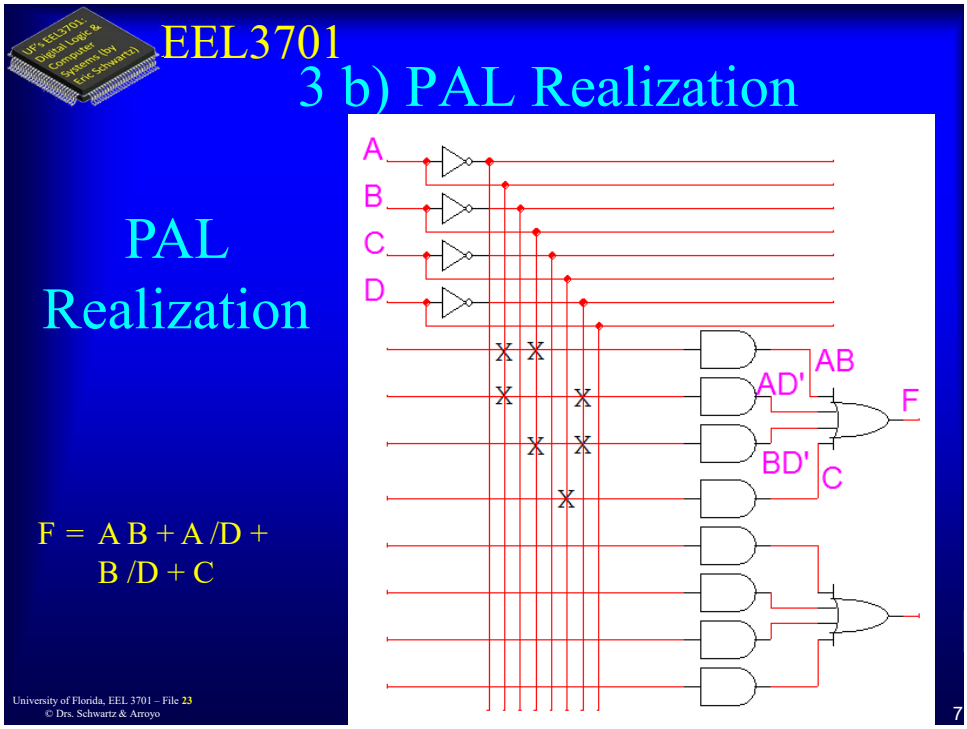
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3 b) PAL Realization
PAL Realization
F = A B + A /D + B /D + C
A
B
C
D
AB
AD'
BD'
C
F
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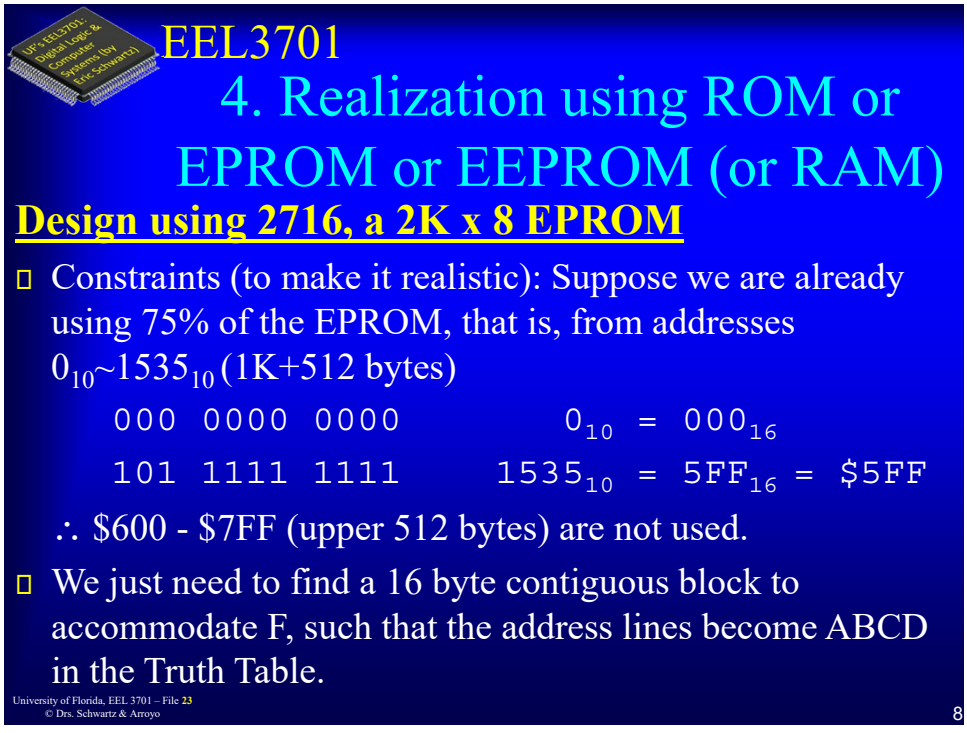
EEL3701
4. Realization using ROM or EPROM or EEPROM (or RAM)
Design using 2716, a 2K x 8 EPROM
Constraints (to make it realistic): Suppose we are already using 75% of the EPROM, that is, from addresses 0_{10}~1535_{10} (1K+512 bytes)
000 0000 0000 0_{10} = 000_{16}
101 1111 1111 1535_{10} = $5FF_{16}$ = $5FF
∴ $600 - $7FF (upper 512 bytes) are not used.
We just need to find a 16 byte contiguous block to accommodate F, such that the address lines become ABCD in the Truth Table.
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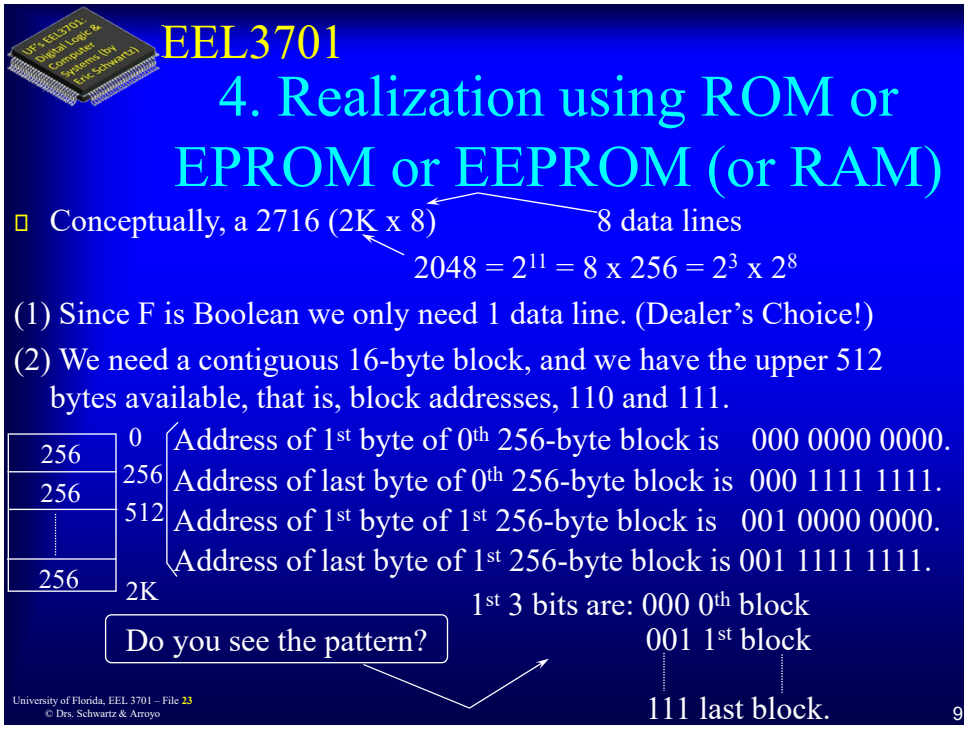
EEL3701
4. Realization using ROM or EPROM or EEPROM (or RAM)
Conceptually, a 2716 (2K x 8)
8 data lines
2048 = 2^11 = 8 x 256 = 2^3 x 2^8
(1) Since F is Boolean we only need 1 data line. (Dealer's Choice!)
(2) We need a contiguous 16-byte block, and we have the upper 512 bytes available, that is, block addresses, 110 and 111.
256
256
256
0
256
512
2K
Address of 1st byte of 0th 256-byte block is 000 0000 0000.
Address of last byte of 0th 256-byte block is 000 1111 1111.
Address of 1st byte of 1st 256-byte block is 001 0000 0000.
Address of last byte of 1st 256-byte block is 001 1111 1111.
Do you see the pattern?
1st 3 bits are: 000 0th block
001 1st block
111 last block.
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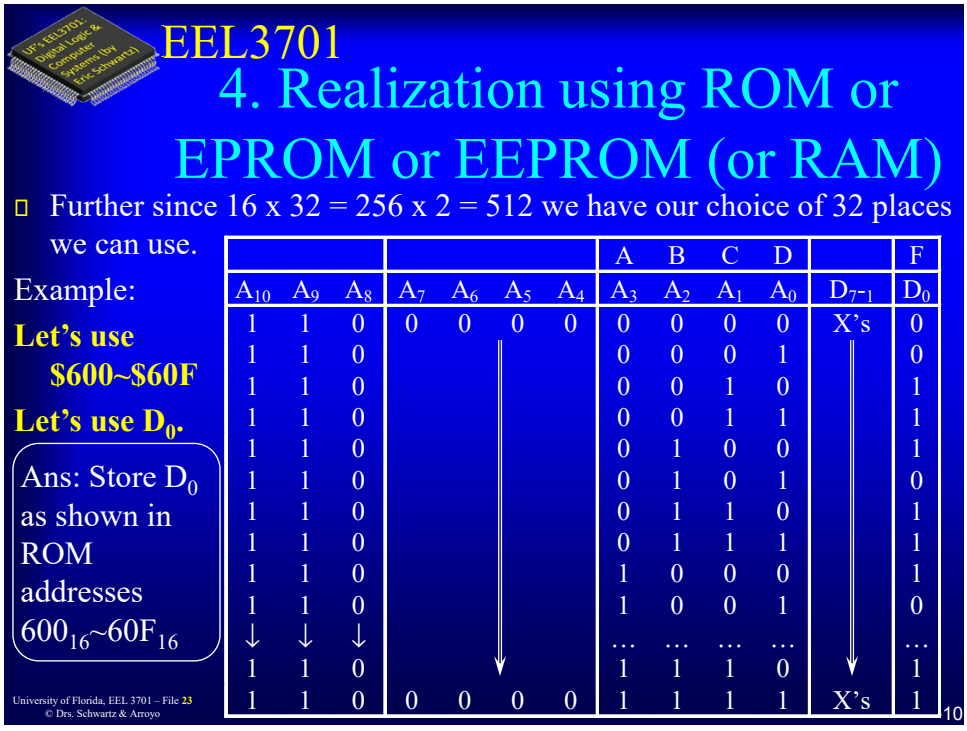
EEL3701
4. Realization using ROM or EPROM or EEPROM (or RAM)
Further since 16 x 32 = 256 x 2 = 512 we have our choice of 32 places we can use.
Example:
Let's use $600~$60F
Let's use D0.
Ans: Store D0 as shown in ROM addresses 600_16~60F_16
A B C D
A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D7-1 D0 F
1 1 0 0 0 0 0 0 0 0 0 X's 0
1 1 0 0 0 0 1 X's 0
1 1 0 0 0 1 0 1
1 1 0 0 0 1 1 1
1 1 0 0 1 0 0 1
1 1 0 0 1 0 1 0
1 1 0 0 1 1 0 1
1 1 0 0 1 1 1 1
1 1 0 1 0 0 0 1
1 1 0 1 0 0 1 0
1 1 0 1 1 1 1 X's 1
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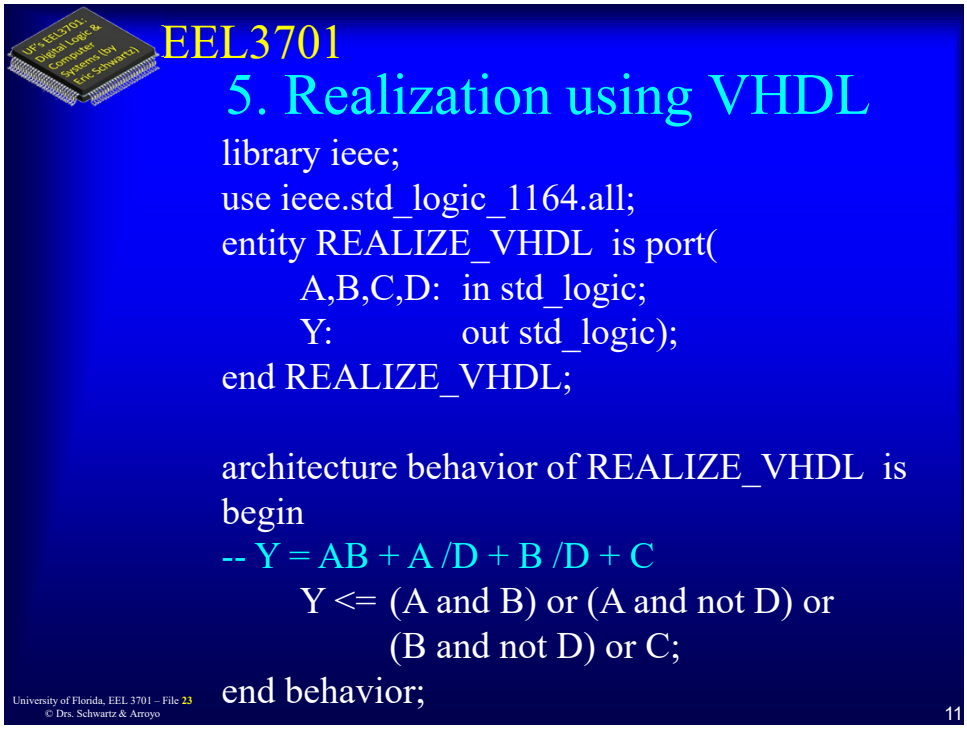
EEL3701
5. Realization using VHDL
library ieee;
use ieee.std_logic_1164.all;
entity REALIZE_VHDL is port(
A,B,C,D: in std_logic;
Y: out std_logic);
end REALIZE_VHDL;
architecture behavior of REALIZE_VHDL is
begin
-- Y = AB + A /D + B /D + C
Y <= (A and B) or (A and not D) or
(B and not D) or C;
end behavior;
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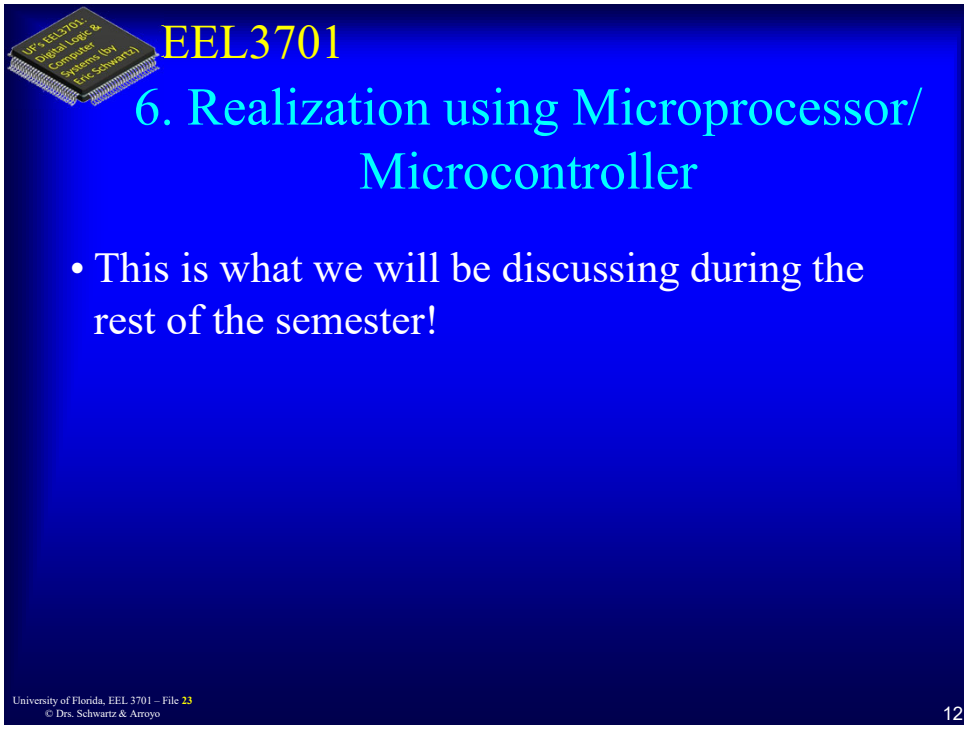
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6. Realization using Microprocessor/ Microcontroller
• This is what we will be discussing during the rest of the semester!
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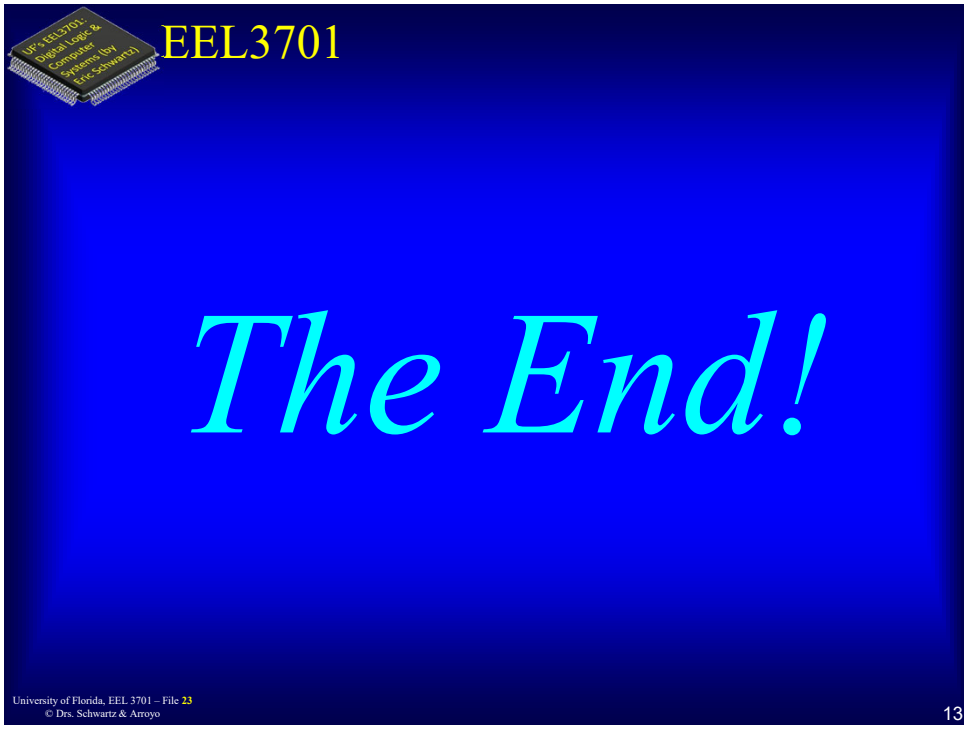
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The End!
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